DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 7/26/2010.

The instant application having Application No. 10/581,873 has a total of 14 claims pending in the application, there are 2 independent claims and 12 dependent claims, all of which are ready for examination by the examiner.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

In light of the amendments made after the Examiner initiated interview on 10/19/2010, the rejections of claims 1-14 have been withdrawn.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Reitseng Lin (Reg #42,804) on 20 October 2010.

The application has been amended as follows:

- Amend page 8, Line 19 of the specification as follows:
  - --granted priority over the AMBA ~~ARAM~~ access operations in—

- Amend page 11, Line 26 of the specification as follows:
  - --command with a Read or ~~of~~ Write command is that a Read--
- Amend Claim 1 as follows:
  - --A method for communication between an IC (integrated circuit) and an external RAM (random access memory), where the external RAM has at least one memory bank and communication between the IC and the external RAM is performed via two or more channels, at least one of the channels is one of a dedicated input and output channel ~~a channel is defined by its physical characteristics regarding at least throughput and latency~~, where data exchange between the IC and the external RAM necessitates at least two memory bank commands, the method comprising:
    receiving ~~transmitting~~ the at least two memory bank commands via multiple channels;
    prioritizing the at least two received ~~transmitted~~ memory bank commands on the basis of a static priority allocation; and
    further prioritizing the at least two commands having the same static priority on the basis of a dynamic priority allocation for the channels.--
- Amend Claim 2 as follows:
  - – The method according to Claim 1, wherein the prioritizing the at least two received ~~transmitted~~ memory bank

commands on the basis of a static priority allocation includes:
giving a 'Burst Terminate' command the highest priority,
giving a 'Read' or 'Write' command the second highest priority,
giving an 'Activate' command the third highest priority, and
giving a 'Precharge' command the lowest priority. –

- Amend Claim 12 as follows:
  - --The method according to Claim 1, wherein the method further includes using a plurality of RAM modules and receiving ~~transmitting~~ a chip enable signal in order to select the desired module.--
- Amend Claim 13 as follows:
  - -- A memory controller for an IC (integrated circuit) with an external RAM (random access memory), where the external RAM has at least one memory bank and communication between the IC and the external RAM is performed via two or more channels, at least one of the channels is one of a dedicated input and output channel ~~a channel is defined by its physical characteristics regarding at least throughput and latency~~, where data exchange between the IC and the external RAM necessitates at least two memory bank commands, the memory controller comprising:
    a command scheduler which prioritizes transmissions of the at least two memory bank commands of multiple channels on the basis of a

static priority allocation for commands and the commands having the same priority are further prioritized by the command scheduler on the basis of a dynamic priority allocation for the channels. --

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references include:

Novak et al (US 6,360,305) teaches a memory controller controlling pre-charge operations.

Novak et al (US 6,046,952) teaches a memory controller controlling refresh operations.

CLOSING COMMENTS

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

SUBJECT MATTER CONSIDERED ALLOWABLE

Claims 1-14 are considered patentably distinguishable over the prior art of

record.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M. A. G./

Examiner, Art Unit 2185

10/21/2010

/Stephen Elmore/
Primary Examiner, Art Unit 2185